What is claimed is:

1. An electron beam exposure mask comprising:

a main mask having a plurality of first defined masks; and

one or more compensation masks including one or more non-

5 defective second defined masks each having a pattern

configuration to be formed in a defective among said first

defined masks.

2. The electron beam exposure mask according to claim 1,

wherein said main mask and at least one compensation mask are

10 arranged on the same substrate.

3. The electron beam exposure mask according to claim 1,

wherein said compensation mask includes one or more non-defective

third defined masks each having a pattern configuration to be

formed in part of said first defined masks irrespective of the

15 presence or absence of a defective among said first defined masks.

4. The electron beam exposure mask according to claim 3,

wherein said compensation mask includes a plurality of

identically patterned defined masks.

5. The electron beam exposure mask according to claim 3,

20 wherein said second defined masks are arranged adjacent to said

main mask.

6. The electron beam exposure mask according to claim 3,

wherein said second defined masks are arranged in the periphery

of said main mask.

25 7. The electron beam exposure mask according to claim 1,

wherein the electron beam exposure mask constitutes a membrane

mask or a stencil mask.

8. An electron beam exposure method comprising the step of

performing an exposure by using the electron beam exposure mask according to claim 1, a first defined mask being used when said first defined mask is non-defective, and said second defined mask corresponding to said first defined mask being used when said

5   first defined mask is defective.

9. An electron beam exposure method comprising the steps of:

recording the address of a defective first defined mask in a main mask having a plurality of first defined masks;

10   recording the address of a second define mask corresponding to said defective first defined mask, in a compensation mask including one or more non-defective second masks each having a pattern configuration to be formed in a defective among said first defined masks; and,

15   when the address of said defective first defined mask is designated, replacing it with the address of said second defined mask corresponding to said first defined mask.

10. A method of fabricating a semiconductor device comprising the steps of:

20   forming an electron beam resist film on a surface of a semiconductor substrate; and

performing an exposure on said electron beam resist film by the method according to claim 8.

11. A method of fabricating a semiconductor device

25   comprising the steps of:

forming an electron beam resist film on a surface of a semiconductor substrate; and

performing an exposure on said electron beam resist film

by the method according to claim 9.

12. An electron beam exposure apparatus comprising:

an electron gun which emits an electron beam;

a mask stage on which an electron beam exposure mask for

5   intercepting part of said electron beam is placed, said electron

beam exposure mask including

a main mask having a plurality of first defined

masks, and

one or more compensation masks including one or more

10   non-defective second defined masks each having a pattern

configuration to be formed in a defective among said first

defined masks;

a wafer stage on which a wafer provided with an electron

beam resist film is placed;

15   a first electron beam optical system which projects said

electron beam onto said electron beam exposure mask;

a second electron beam optical system which projects said

electron past said electron beam exposure mask onto said electron

beam resist film;

20   a storage device which stores the address of a defective

among said first defined mask and the address of a second defined

mask corresponding to said first defined mask; and

a control device which controls the deflection of said

electron beam in said first and second electron beam optical

25   systems, said control device, when the address of said defective

first defined mask is designated, replacing it with the address

of said second defined mask corresponding to said first defined

mask.